Notice of Allowability	Application No.	Applicant(s)	
	10/779,752	TAKAHASHI, AKIRA	
	Examiner	Art Unit	
	Thanhha Pham	2813	
The MAILING DATE of this communication appe All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RI of the Office or upon petition by the applicant. See 37 CFR 1.313	(OR REMAINS) CLOSED in this ap or other appropriate communication GHTS. This application is subject to	plication. If not include will be mailed in due	ed course. THIS
1. X This communication is responsive to 02/18/2004 and interv	riews dated 04/12/2005 & 04/14/200	<u>)5</u> .	
2. The allowed claim(s) is/are 9,11,12 and 15-17.	•	·	
3. \boxtimes The drawings filed on <u>18 February 2004</u> are accepted by the	ne Examiner.		
 4. Acknowledgment is made of a claim for foreign priority una) All b) Some* c) None of the: 1. Certified copies of the priority documents have 2. Certified copies of the priority documents have 3. Copies of the certified copies of the priority documents have International Bureau (PCT Rule 17.2(a)). * Certified copies not received: Applicant has THREE MONTHS FROM THE "MAILING DATE" on oted below. Failure to timely comply will result in ABANDONM THIS THREE-MONTH PERIOD IS NOT EXTENDABLE. 	been received. been received in Application No. <u>O</u> cuments have been received in this	national stage applica	
5. A SUBSTITUTE OATH OR DECLARATION must be submit INFORMAL PATENT APPLICATION (PTO-152) which give			NOTICE OF
 6. CORRECTED DRAWINGS (as "replacement sheets") mus (a) including changes required by the Notice of Draftspers 1) hereto or 2) to Paper No./Mail Date (b) including changes required by the attached Examiner's Paper No./Mail Date ldentifying indicia such as the application number (see 37 CFR 1. each sheet. Replacement sheet(s) should be labeled as such in the depose attached Examiner's comment regarding REQUIREMENT for the depose attached Examiner's comment regarding for the depose attached Examiner's comment for the depose attached Examiner's comment for the depose attached Examiner's comment for t	on's Patent Drawing Review (PTO- s Amendment / Comment or in the C 84(c)) should be written on the drawing the header according to 37 CFR 1.121(sit of BIOLOGICAL MATERIAL r	Office action of ngs in the front (not the d).	·
Attachment(s) 1. ☑ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) 3. ☑ Information Disclosure Statements (PTO-1449 or PTO/SB/0 Paper No./Mail Date 02/18/2004 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	5. Notice of Informal F 6. Interview Summary Paper No./Mail Da 8), 7. Examiner's Amenda 8. Examiner's Statema 9. Other	(PTO-413), te ment/Comment	·

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EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Andrew Telesz on 04/12/2005 and 04/14/2005.

The application has been amended as follows:

In claim 9,

line 30, delete "over a wide area"

In claim 12,

line 6, change "tetraethylorthosilicate" to - silane -

In claim 16,

line 4, change "tetraethylorthosilicate glass" to – tetraethylorthosilicate – line 5, change "tetraethylorthosilicate glass" to – silane –

In specification, the paragraph beginning on line 14 of page 25,

line 3, change "using tetraethylorthosilicate glass" to -- using tetraethylorthosilicate --

Allowable Subject Matter

2. Claims 9, 11-12 and 15-17 are allowed.

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The following is an examiner's statement of reasons for allowance: Recorded 3. Prior Art fails to disclose or suggest the combination of the process steps for manufacturing a semiconductor device as recited in the base claim 9 including successively etching said silicon nitride layer and said lower side wall spacers precursor layer so as to form side wall spacers having a structure consisting of upper side wall spacer portions and lower side wall spacer portions, said upper side wall spacer portions being formed of said silicon nitride layer remaining on upper side walls of gate electrodes, and said lower side wall spacer portions being formed of said silicon oxide layer remaining on lower side walls of said gate electrodes wherein said forming a plurality of gate electrodes comprises forming said gate electrodes so as to provide a dense region where said gate electrodes are densely gathered and a sparse region where said gate electrodes are more scattered, so that a film thickness of said silicon. oxide layer in said dense region is greater than a film thickness of said silicon oxide layer in said sparse region, the method further comprising performing chemical mechanical polishing to smooth out the silicon oxide layer prior to said forming a lower side wall spacer precursor layer. Recorded Prior Art also fails to disclose or suggest the combination of the process steps for manufacturing a semiconductor device as recited in the base claim 15 including forming a silicon oxide layer so as to cover the substrate and the first and second gate electrodes, a film thickness of said silicon oxide layer in the first region is greater than a film thickness of said silicon oxide layer in the second region; performing chemical mechanical polishing to smooth out said silicon oxide layer; forming a lower side wall spacer precursor layer that is thinner than the first and

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second gate electrodes by etching said silicon oxide layer, after said performing chemical mechanical polishing; forming a silicon nitride layer so as to cover the lower side wall spacer precursor layer; and successively etching the silicon nitride layer and the lower side wall spacer precursor layer so as to form side wall spacers having a structure consisting of first and second upper side wall spacer portions and first and second lower side wall spacer portions, the first upper side wall spacer portions being formed of said silicon nitride layer on upper side walls of the first gate electrodes, the first lower side wall spacer portions being formed of said silicon oxide layer on lower side walls of the first gate electrodes, the second upper side wall spacer portions being formed of said silicon nitride layer on upper side walls of the second gate electrodes, and the second lower side wall spacer portions being formed of said silicon oxide layer on lower side walls of the second gate electrodes.

- 4. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."
- 5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanhha Pham whose telephone number is (571) 272-1696. The examiner can normally be reached on Monday and Thursday 9:00AM 9:30PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thanhha Pham

CRAIG A. THOMPSON PRIMARY EXAMINER